Patent

Customer No. 31561
Docket No. 13464-US-PA
Application No.: 10/711,380

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Yen-Chang Tung
Application No.	: 10/711,380
Filed	: September 15, 2004
For	: VOLTAGE CONTROLLED OSCILLATOR WITH TEMPERATURE AND PROCESS COMPENSATION
Examiner	: JOSEPH CHANG
Art Unit	: 2817

TRANSMITTAL LETTER
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(Via fax: 1+15 pages)

Ms. TRACEY YOUNG
PATENT APPEAL CENTER
United States Patent and Trademark Office
Alexandria, VA 22314

Dear Ms. Young,

In response to the Notification of Non-Compliant Appeal Brief (37 CFR 41.37) mailed on January 10, 2007, please find the relevant paper in response thereto as follows:

- Supplementary Appeal Brief in (15) pages.

The Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No.: 50-2620 (Order No.:13464-US-PA).

Thank you for your attention and assistance in this matter. Should you have any questions, please feel free to contact the undersigned.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: Feb. 12, 2007

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE Yen-Chang Tung

Application for Patent

Filed: September 15, 2004

Serial No. 10/711,380

FOR:

VOLTAGE CONTROLLED OSCILLATOR WITH TEMPERATURE AND PROCESS COMPENSATION

(as amended)

AMENDED APPEAL BRIEF

JIANQ CHYUN Intellectual Property Office
Representative for Applicants

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Yen-Chang Tung, the inventor named in the subject application, and SUNPLUS TECHNOLOGY CO. LTD., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

Claims 1-16 are pending. Specifically, claims 1, 3, 4, 16 were finally rejected under 35 U.S.C. 102(b), as being anticipated by Jelinek et al. (US Patent 5,331,295), and claims 2, 5-15 are finally rejected under 35 U.S.C. 103(a) as being unpatentable over Jelinek et al. (US Patent 5,331,295) in view of Klughart (US Patent 5,798,669).

This appeal involves all the finally rejected claims 1-16.

IV. Status of amendments

There is no amendment after final rejection.

V. Summary of claimed subject matter

The claimed subject matter of independent claim 1 involved in the appeal is directed to a voltage control oscillator for outputting a clock signal with a frequency according to an input voltage (as shown in FIG.2A and as discussed in Lines 3~17 of Para. [0029] and in Lines 1-12 of Para. [0030]). The voltage control oscillator, as shown in FIG 2A, includes a constant current source ("CS" in FIG.2A), a voltage/ current converter ("220" in FIG.2A), a current mirror ("CM" in FIG.2A) and an oscillating circuit ("230" in FIG.2A). The constant current source is used for providing a reference current ("I" in FIG.2A and Lines 5-6 of Para. [0029]). The voltage/ current converter, coupled to the constant current source, is used for

determining a first current passing through the voltage/ current converter according to the input voltage (Lines 8-11 of Para. [0029]). The current mirror, having a first current terminal and a second current terminal, the first current terminal being coupled to the constant current source, is used for determining a third current passing through the second current terminal according to the second current passing through the first current terminal, wherein the second current is the reference current subtracted by the first current (Lines 11-19 of Para. [0029]). The oscillating circuit, coupled to the second current terminal of the current mirror, is used for determining the frequency of the outputted clock signal according to the third current (Lines 1-3 of Para. [0030]).

Dependent claims 2-16 provide more details about the preferred embodiments discussed in association with the drawings Figs. 2A through 4.

VI. Grounds of rejection to be reviewed on appeal

A. **Were claims 1, 3, 4 and 16 properly rejected under 35 U.S.C. 102(b) as being anticipated by Jelinek (U.S. Pat. No. 5,331,295, hereinafter "Jelinek")**

B. **Were claims 2 and 5-15 properly rejected under 35 U.S.C. 103(a) as being unpatentable over by Jelinek in view of Klughart (U.S. Pat. No. 5,798,669, hereinafter "Klughart")**

VII. Arguments

A. The related laws

In order to properly anticipate Applicants' claimed invention under 35 U.S.C.§ 102(b), each and every element of the claim in issue must be found "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown as complete detail as is contained in the ...claim Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P § 2131, 8th ed., 2001.

The standard for lack of novelty is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. ..... These elements must be arranged as in the claim under review. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides : That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, **by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation.** Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." MPEP § 2143, 8th ed., February 2003.

A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C § 103(a); see *Graham v. John Deere Co.*, 383 U.S. 1, 14, 86 S. Ct. 684, 15 L.Ed.2d 545, 148 USPQ 459, 465 (1966).

"The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness International, Inc. Vs. Simplimatic Engineering Co., 819 F2d 1100, 1108, 2 USPQ 2D 1826 (Fed. Cir. 1987).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

"Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blue print for piecing together the prior art to defeat patentability—the essence of hindsight". *In re Dembiczak*, 175 F.3d at 999.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from the references to fill the gaps". *In re Gorman*, 933 F. 2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

B. Grouping of the claims

For the ground of rejection contested by appellant in this appeal, claims 1-15 are treated as one group to stand or fall together. Claim 1, the independent claim pending, may be taken as representative for the issues on appeal.

C. Claims 1, 3, 4 and 16 were improperly rejected under 35 U.S.C. 102(b) as being anticipated by Jelinek (U.S. Pat. No. 5,331,295, hereinafter "Jelinek")

The Examiner rejected claims 1, 3, 4 and 16 as being anticipated by Jelinek.

Applicant respectfully disagrees with such assertion in the Office Action that Jelinek shows all the limitations of the instant invention as defined in claims 1, 3, 4 and 16.

In responsive to the rejections, Appellant submitted that what the Examiner alleged that "the reference current 12 is the sum of the first current and the second current and because of current mirror, the third current (138) is approximately equal to the second current" in the first nonfinal Office Action dated Nov. 23, 2005, and recited in the final Office Action dated May 2, 2006 is improper.

In supporting the aforementioned statement, the Examiner had previously interpreted current through left side of 16 of Jelinek as reading on the first current, current through right side of 16 of Jelinek as reading on the second current, and current through 138 of Jelinek as reading on the third current. However, as set forth in claim 1, "a voltage/ current converter, coupled to the constant current source, for determining a first current passing through the voltage/ current converter" (Emphasis added). Appellant submits that the first current should not be arbitrarily designated to any by the Examiner, because it has been defined as passing through the voltage/current converter. It is easy to identify that a left side of a converter is clearly not the converter itself, and also a current through a left side of a converter or the like is clearly not the current passing through the converter. Therefore, current through left side of 16 of Jelinek does not read on the first current as required by claim 1.

Further, Appellant submits that whatever the first current be interpreted as being read on by any of Jelinek, there is no evidence could be found from Jelinek or provided by the Examiner that "the reference current 12 is the sum of the first current and the second current" as the Examiner stated in the Office Actions. On the contrary, Jelinek teaches: "[T]he connection of the two current sources at node 90 in attenuator 16 results in the supply current provided to attenuator 16 being the output of the second current source (14) subtracted from the output of the first current source (col. 4, lines 14-18). Appellant submits that the current of the second current source 14 of Jelinek that involved in the equation does not satisfy the limitation of the first current, i.e., "passing through the voltage/current converter". Only when after combined with the reference current provided by the first current source 12, current from the second current source of Jelinek can reach and thereafter pass through the alleged voltage/current converter.

As a result, claims 1, 3, 4 and 16 are patentable over Jelinek.

D. Claims 2 and 5-15 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over by Jelinek in view of Klughart (U.S. Pat. No. 5,798,669, hereinafter "Klughart")

The Examiner rejected Claims 2 and 5-15 under 35 U.S.C. 103(a) as being unpatentable over by Jelinek in view of Klughart.

Applicant respectfully submits that claims 2-16 depend on allowable independent claim 1, and thus should also be allowable.

E. The Examiner failed to answer all material traversed during the prosecution history.

Responsive to Reply, Appellant filed on Jul. 31, 2006, and all arguments submitted therewith, The Examiner asserted that "The various new issue amended in the claims requires further consideration". Appellant submits that there was no amendment to the claims at all submitted. Due to the Examiner's arbitrary decisions and possible oversight, Appellant has lost his right granted by the US law system to have his application reconsidered before going to the appeal procedure and within the statutory period. At the same time, prosecution is also unfortunately prolonged. During a telephone interview between the Examiner and Appellant's representative dated Aug. 27, 2006, the Examiner admitted that "The previous Advisory Action of 8/14/06 was improperly indicated on Box 3". However, the Examiner further stated that "The indication should have been checked on Box 11 with the following statement: -- The arguments are not persuasive". As held in MPEP §707.07(f), "an examiner must provide clear explanations of all actions taken by the examiner during prosecution of an application", and "[W]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it". Appellant submits that the Examiner failed to answer all material traversed during the prosecution history, especially he repeated previous rejections without giving any explanation on why the arguments are not persuasive. Appellant submits that such an Advisory Action had been improperly made and corrected later in the telephone interview. Unanswered arguments presented in Appellant's last Reply are listed as below for the board's reference:

"(a) Applicant does not agree that the disclosures of FIG.1 of the Jelinek reference have anticipated that "a constant current source, for providing a reference current, ... wherein the second current is the reference current subtracted by the first current" as claimed in claim 1. Instead, in the Jelinek reference, the reference current means the current for the attenuator 16 (the sum of the first split current passing through left transistor of 16 and the second split current passing through right transistors of 16) and is obtained by subtracting the variable second current provided by the second current source 14 from the constant first current provided by the first current source 12. Thereof, Jelinek et al. does not anticipate that "a constant current source, for providing a reference current..... wherein the second current is the reference current subtracted by the first current" as claimed in claim 1;

(b) the Office Action asserted that "the difference between Attenuator 16 and V-I converter 220 of this application has no bearing on the scope of the claim." However, in the previous argument, Applicant emphasized that "the second split current passing through right transistors of 16 is obtained by comparing the input voltage Vfilter 20 to the reference voltage Vref", which is different from the invention that "a voltage/ current converter, coupled to the constant current source, for determining a first current passing through the voltage/ current converter according to the input voltage" as claimed in claim 1. The argument is bearing on the scope of the claim."

F. Conclusion

In view of the above discussion, Applicant believes that the rejections under 35 U.S.C. 102 and 35 U.S.C. 103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,

Date : Feb. 12, 2007

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VIII. Claims appendix

CLAIMS ON APPEAL:

1. (original) A voltage control oscillator, for outputting a clock signal with a frequency according to an input voltage, comprising:

a constant current source, for providing a reference current;

a voltage/ current converter, coupled to the constant current source, for determining a first current passing through the voltage/ current converter according to the input voltage;

a current mirror, having a first current terminal and a second current terminal, the first current terminal being coupled to the constant current source, for determining a third current passing through the second current terminal according to the second current passing through the first current terminal, wherein the second current is the reference current subtracted by the first current; and

an oscillating circuit, coupled to the second current terminal of the current mirror, for determining the frequency of the outputted clock signal according to the third current.

2. (original) The VCO as recited in claim 1, wherein the oscillating circuit comprises:

a current control oscillator, coupled to the second current terminal of the current mirror, for receiving and determining the frequency according to the third current and outputting a pulse signal having the frequency; and

a wave shaping circuit, coupled to the current control oscillator, for shaping the pulse signal to the clock signal having a specific wave shape.

3. (original) The VCO as recited in claim 1, wherein the constant current source has a reference current input terminal and a reference current output terminal, wherein the reference current output terminal is coupled to a ground voltage level, the reference input terminal is coupled to and receives the first current outputted from the voltage/ current

converter and the second current outputted from the first current terminal of the current mirror.

4. (original) The VCO as recited in claim 3, wherein the current mirror comprises:

a first P-type transistor, wherein a source of the first P-type transistor is coupled to a system voltage, a gate of the first P-type transistor is coupled to a drain of the first P-type transistor and the reference current input terminal; and

a second P-type transistor, a source of the second P-type transistor is coupled to the system voltage, a gate of the second P-type transistor is coupled to the gate of the first P-type transistor, a drain of the second P-type transistor is coupled to the oscillating circuit.

5. (original) The VCO as recited in claim 3, wherein the voltage/ current converter comprises a third P-type transistor, a gate of the third P-type transistor receives the input voltage, a source of the third P-type transistor is coupled to the system voltage, a drain of the third P-type transistor is coupled to the reference current input terminal and outputting the first current.

6. (original) The VCO as recited in claim 5, wherein a body of the third P-type transistor is coupled to the source of the third P-type transistor.

7. (original) The VCO as recited in claim 5, wherein the voltage/ current converter further comprises a resistor, wherein the resistor is coupled between the system voltage and the source of the third P-type transistor.

8. (original) The VCO as recited in claim 7, wherein the voltage/ current converter further comprises an operational amplifier coupled between the input voltage and the gate of the third P-type transistor, wherein a positive terminal of the operational amplifier receives the input voltage, a negative terminal of the operational amplifier is coupled to the source of the third P-type transistor, and an output terminal of the operational amplifier is coupled to the gate of the third P-type transistor.

9. (original) The VCO as recited in claim **3**, further comprising a fourth P-type transistor coupled between the first current terminal of the current mirror and the reference current input terminal, wherein a source of the fourth P-type transistor is coupled to the first current terminal of the current mirror, a gate of the fourth P-type transistor is coupled to a drain of the fourth P-type transistor and the reference current input terminal.

10. (original) The VCO as recited in claim **1**, wherein the constant current source has a reference current input terminal and a reference current output terminal, wherein the reference current input terminal is coupled to the system voltage, the reference current output terminal is coupled to the voltage/ current converter and the first current terminal of the current mirror.

11. (original) The VCO as recited in claim **10**, wherein the current mirror comprises:

a first N-type transistor, a source of the first N-type transistor is coupled to the ground voltage level, a gate of the first N-type transistor is coupled to a drain of the first N-type transistor and the reference current output terminal; and

a second N-type transistor, a source of the second N-type transistor is coupled to the ground voltage level, a gate of the second N-type transistor is coupled to the gate of the first N-type transistor, and a drain of the second N-type transistor is coupled to the oscillating circuit.

12. (original) The VCO as recited in claim **10**, wherein the voltage/ current converter comprises a third n-type transistor, a gate of the third n-type transistor is coupled to the input voltage, a source of the third N-type transistor is coupled to the ground voltage level, a drain of the third N-type transistor is coupled to the reference current output terminal for accommodating the first current.

13. (original) The VCO as recited in claim **12**, wherein the voltage/ current converter further comprises a resistor, and the resistor is coupled between the source of the third N-type transistor and the ground voltage level.

14. (original) The VCO as recited in claim **13**, wherein the voltage/ current converter further comprises an operational amplifier coupled between the input voltage and the gate of the third N-type transistor, wherein a positive input terminal of the operational amplifier receives the input voltage, a negative input terminal of the operational amplifier is coupled to the source of the third N-type transistor, an output terminal of the operational amplifier is coupled to the gate of the third N-type transistor.

15. (original) The VCO as recited in claim **10**, further comprising a fourth N-type transistor coupled between the first current terminal of the current mirror and the reference current output terminal, wherein a source of the fourth N-type transistor is coupled to the first current terminal of the current mirror, a gate of the fourth N-type transistor is coupled to a drain of the fourth N-type transistor and the reference current output terminal.

The VCO as recited in claim **1**, wherein the third current is approximately equal to the second current.

IX. Evidence appendix

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

X. Related proceedings appendix

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.